

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FII	JING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,234	12/27/2000		Linden Minnick	10559-386001 / P10193	6622
20985	7590	11/29/2004		EXAM	INER
FISH & RIC 12390 EL C		,	PHAN, TAM T		
SAN DIEGO, CA 92130-2081			ART UNIT	PAPER NUMBER	
				2144	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
	09/750,234	MINNICK, LINDEN
Office Action Summary	Examiner	Art Unit
	Tam (Jenny) Phan	2144
The MAILING DATE of this communicated for Reply	ation appears on the cover shee	t with the correspondence address
A SHORTENED STATUTORY PERIOD FOR THE MAILING DATE OF THIS COMMUNIC. - Extensions of time may be available under the provisions of after SIX (6) MONTHS from the mailing date of this commun. - If the period for reply specified above is less than thirty (30) of the period for reply is specified above, the maximum statut. - Failure to reply within the set or extended period for reply will Any reply received by the Office later than three months after earned patent term adjustment. See 37 CFR 1.704(b).	ATION. 37 CFR 1.136(a). In no event, however, ma ication. days, a reply within the statutory minimum of ory period will apply and will expire SIX (6) I, by statute, cause the application to becom	y a reply be timely filed f thirty (30) days will be considered timely. MONTHS from the mailing date of this communication. e ABANDONED (35 U.S.C. § 133).
Status		
 1) Responsive to communication(s) filed 2a) This action is FINAL. 3) Since this application is in condition fo closed in accordance with the practice)⊠ This action is non-final. r allowance except for formal m	•
Disposition of Claims		•
4) Claim(s) 1,3-12,14-22 and 24-32 is/are 4a) Of the above claim(s) is/are 5) Claim(s) is/are allowed. 6) Claim(s) 1,3-12,14-22 and 24-32 is/are 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction Application Papers 9) The specification is objected to by the 10	withdrawn from consideration. e rejected. on and/or election requirement. Examiner. 2000 is/are: a) accepted or both to the drawing(s) be held in abelie correction is required if the drawing the	o) objected to by the Examiner. eyance. See 37 CFR 1.85(a). ving(s) is objected to. See 37 CFR 1.121(d).
Priority under 35 U.S.C. § 119	,	
12) Acknowledgment is made of a claim fo a) All b) Some * c) None of: 1. Certified copies of the priority do 2. Certified copies of the priority do	ocuments have been received. Ocuments have been received in the priority documents have been large (PCT Rule 17.2(a)).	n Application No een received in this National Stage
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-3) Information Disclosure Statement(s) (PTO-1449 or PT Paper No(s)/Mail Date	D-948) Paper	ew Summary (PTO-413) No(s)/Mail Date of Informal Patent Application (PTO-152)

Application/Control Number: 09/750,234 Page 2

Art Unit: 2144

DETAILED ACTION

1. Amendment received on 07/26/2004 has been entered. Claims 1, 12, 22 are currently amended. Claims 2, 13, 23 are cancelled. Claims 30-32 are new. Claims 3-11, 14-21, 24-29 are previously presented.

2. Claims 1, 3-12, 14-22, and 24-32 are presented for examination.

Priority

- 3. No priority claims have been made.
- 4. The effective filing date for the subject matter defined in the pending claims in this application is 12/27/2000.

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 1, 5-7, 12, 16-18, 22, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pickreign et al. (U.S. Patent Number 6,732,246), hereinafter referred to as Pickreign, in view of Sharma et al. (U.S. Patent Number 6,647,469), hereinafter referred to as Sharma.
- 7. Regarding claim 1, Pickreign disclosed a method comprising allocating space in a host, memory for use as a buffer (Figures 1 & 3, column 1 lines 41-56, column 2 lines 5-9); copying contents of a memory of a network interface controller into the buffer (Figures 1 & 3, column 1 lines 41-56, column 2 lines 5-9,

claim 1); and accessing the buffer in response to a request for information in the network interface controller memory (column 6 lines 46-63, column 7 lines 41-44).

- 8. Pickreign taught the invention substantially as claimed. However, Pickreign did not expressly teach updating [modifying] the contents of the network interface controller memory and correspondingly updating [modifying] the contents of the buffer [data coherency].
- 9. Pickreign suggested exploration of art and/or provided a reason to modify the method for accessing information from memory with additional features (column 7 lines 46-50).
- 10. Sharma disclosed a method of updating [modifying] the contents of the network interface controller memory and correspondingly updating [modifying] the contents of the buffer [the memory controller ensures that the data stored in system memory is accurately and precisely mirrored in all subservient copies of that data as might typically be stored in agent cache memories] and [the memory controller implements a first set of rule in the coherent mode of operation to insure that all copies of data stored by the agents are coherent with data stored in the memory] (Abstract, column 3 lines 62-64, column 5 lines 11-17).
- 11. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the method of Pickreign with the teachings of Sharma to include the data coherency feature in order to prevent the content in the buffer from become stale prior to use by the host memory (Sharma, column 3 lines 62-64, column 4 lines 5-9).

- 12. Regarding claim 5, Pickreign disclosed a method further comprising: initializing a physical layer; and subsequently initializing the buffer to store the contents of the network interface controller memory (Figure 3, column 3 lines 50-61, column 6 lines 53-63).
- 13. Regarding claim 6, Pickreign disclosed a method wherein the network interface controller memory comprises an EEPROM (Figure 1, column 1 lines 28-32).
- 14. Regarding claim 7, Pickreign and Shah combined disclosed a method comprising: copying contents of a network interface controller memory into a buffer in host memory (Pickreign, Figures 1 & 3, column 1 lines 41-56, column 2 lines 5-9, claim 1); recopying the contents of the network interface controller memory into the buffer if the contents of the network interface controller memory are modified (Abstract, column 3 lines 62-64, column 5 lines 11-17); and accessing the buffer in response to a request for information in the network interface controller memory (Pickreign, column 6 lines 46-63, column 7 lines 41-44).
- 15. Regarding claims 12 and 16-17, the apparatus corresponds directly to the method of claims 1 and 5-6, and thus these claims are rejected using the same rationale.
- 16. Regarding claim 18, the apparatus corresponds directly to the method of claim 7, and thus is rejected using the same rationale.

- 17. Regarding claims 22 and 26, the article comprising a computer readable medium corresponds directly to the method of claims 1 and 5 and the apparatus of claims 12 and 16, and thus is rejected using the same rationale.
- 18. Regarding claim 27, the article comprising a computer readable medium corresponds directly to the method of claim 7, and thus is rejected using the same rationale.
- 19. Since all the limitations of the claimed invention were disclosed the combination of Pickreign and Sharma, claims 1, 5-7, 12, 16-18, 22, and 26-27 are rejected.
- 20. Claims 3-4, 8-11, 14-15,19-21, 24-25, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pickreign et al. (U.S. Patent Number 6,732,246), hereinafter refer to as Pickreign, in view of Shah et al. (U.S. Patent Number 6,470,397) hereinafter referred to as Shah.
- 21. Regarding claim 3, Pickreign disclosed a method comprising allocating space in a host, memory for use as a buffer; copying contents of a memory of a network interface controller into the buffer; and accessing the buffer in response to a request for information in the network interface controller memory (Figures 1 & 3, column 1 lines 41-56, column 2 lines 5-9, column 6 lines 46-63, column 7 lines 41-44, claim 1).
- 22. Pickreign taught the invention substantially as claimed. However,

 Pickreign did not expressly teach initializing a device driver in a Network Driver

Interface Specification [NDIS] environment to allocate the space in the host memory.

- 23. Fesas suggested exploration of art and/or provided a reason to modify the method with the initializing a device driver in a NDIS environment feature [NDIS miniport is conventional in performing hardware-specific operations needed to manage the Network Interface Card] (Figure 1, column 1 lines 41-56, column 7 lines 46-51).
- 24. Shah disclosed a method comprising initializing a device driver in a Network Driver Interface Specification [NDIS] environment to allocate the space in the host memory (Figures 3 & 5, column 2 lines 24-37, column 6 lines 12-46) in less than a second [Ethernet emulation through multiple enhanced miniport drivers simultaneously] (column 7 lines 11-17).
- 25. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the method of Fesas with the teaching of Shah to include the NDIS feature in order to supports multiple Ethernet emulations (Shah, column 7 lines 11-17) since in conventional system, the NDIS miniport performs the hardware-specific operations needed to manage the Network Interface Card (Shah, column 2 lines 24-37).
- 26. Regarding claim 4, Pickreign and Shah combined disclosed a method comprising initializing the buffer to store the contents of the network interface controller memory wherein initializing the buffer occurs at a different time from the driver initialization (Pickreign, column 1 lines 41-56, column 2 lines 27-34; Shah, column 9 lines 64-67, column 10 lines 1-13, column 11 lines 9-22).

- 27. Regarding claim 8, Pickreign and Shah disclosed a method further comprising initializing a driver to allocate memory space to the buffer (Pickreign, column 1 lines 41-56, column 2 lines 27-34; Shah, column 6 lines 12-26, column 10 lines 4-13).
- 28. Regarding claims 9-10, 19-20, and 28, these limitations are similar to the limitations of claims 3-4, and thus these claims are rejected using the same rationale.
- 29. Regarding claim 11, Pickreign and Shah disclosed a method further comprising initializing the buffer to store the contents of the network interface controller memory in response to a first request to read the contents of the network interface controller memory (Pickreign, column 1 lines 41-55; Shah, Figures 3, 5, column 6 lines 12-26).
- 30. Regarding claims 14-15 and 24-25, the apparatus of claims 14-15 and the computer-readable medium article of claims 24-25 corresponds directly to the method of claims 3-4, and thus these claims are rejected using the same rationale.
- 31. Regarding claims 21 and 29, the apparatus of claim 21 and the computerreadable medium article of claim 29 corresponds directly to the method of claim 11, and thus these claims are rejected using the same rationale.
- 32. Since all the limitations of the claimed invention were disclosed by the combination of Pickreign and Shah, claims 3-4, 8-11, 14-15,19-21, 24-25, and 28-29 are rejected.

- 33. Claims 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pickreign et al. (U.S. Patent Number 6,732,246), hereinafter refer to as Pickreign, in view of in view of Sharma et al. (U.S. Patent Number 6,647,469), hereinafter referred to as Sharma, and further in view of Shah et al. (U.S Patent Number 5,761,417), hereinafter referred to as Shah.
- 34. Regarding claim 30, Pickreign disclosed a method comprising allocating space in a host, memory for use as a buffer (Figures 1 & 3, column 1 lines 41-56, column 2 lines 5-9); copying contents of a memory of a network interface controller into the buffer (Figures 1 & 3, column 1 lines 41-56, column 2 lines 5-9, claim 1); and accessing the buffer in response to a request for information in the network interface controller memory (column 6 lines 46-63, column 7 lines 41-44). Sharma disclosed a method of updating [modifying] the contents of the network interface controller memory and correspondingly updating [modifying] the contents of the buffer (Abstract, column 3 lines 62-64, column 5 lines 11-17).
- 35. The combination of Pickreign and Sharma taught the invention substantially as claimed. However, the combination of Pickreign and Sharma did not expressly teach a step of wherein correspondingly modifying the contents of the buffer occurs independently of a request by a host to access information in the network interface controller memory.
- 36. Sharma suggested exploration of art and/or provided a reason to modify the method for accessing information from memory additional features (column 3 line5 lines 22-34).

Application/Control Number: 09/750,234

Art Unit: 2144

37. Shah disclosed a step of correspondingly modifying the contents of the buffer occurs independently of a request by a host to access information in the network interface controller memory (Abstract, column 2 lines 30-37, column 7 lines 27-44).

Page 9

- 38. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the combined method of Pickreign and Sharma with the teachings of Shah to include a step of correspondingly modifying the contents of the buffer occurs independently of a request by a host to access information in the network interface controller memory in order to ensure consistency and reduce spurious interrupts (Shah, column 2 lines 54-56). The updated data is available for the host to read at its convenient without incur any performance penalties (column 2 lines 56-59).
- 39. Regarding claim 31, the apparatus corresponds directly to the method of claim 30, and thus is rejected using the same rationale.
- 40. Regarding claim 32, the computer-readable medium article corresponds directly to the method of claim 30, and thus is rejected using the same rationale.
- 41. Since all the limitations of the claimed invention were disclosed by the combination of Pickreign, Sharma, and Shah, claims 31-32 are rejected.

Response to Arguments

- 42. Applicant's arguments filed 07/26/2004 with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.
- 43. In response to applicant's particular example take from the pending specification, the examiner is appreciative of applicant's effort to clarify the

claimed limitation. However, the examiner would like to remind the applicant that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

- 44. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).
- 45. As the rejection reads, Examiner asserts that the combination of these teachings render the claimed invention obvious.

Conclusion

- 46. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
 - a. Varada et al. "Data and Buffer Management in ATM Systems" disclosed the handling of data traffic, at an end-user host or access in a high speed Asynchronous Transfer Mode (ATM) network environment.

 From the reasons of cost and space, on a network adapter card, often ASICs rely upon the host for data buffers in the host memory in addition to control and configuration. Such reliance places demand on the host

memory and requires a data and buffer management mechanism that provides a framework for optimization of the memory utilization and data packet latency. The method details a buffer management mechanism wherein the host buffers are allocated in the host memory during system initialization.

- b. Gentry (EP 775958 A1) titled "Mechanism for reducing data copying overhead in protected memory operating systems" disclosed a method and an apparatus for reducing data copying overhead associated with protected memory operating systems. The present invention's NIC (network interface circuit) demultiplexes the information in the header of the incoming packet and routes the packet directly to its final destination using the present invention's concept of targeted buffer rings. Thus, instead of having the packet be DMA'd to a buffer in a descriptor ring in the kernel, it may be routed directly to the buffer ring of the destination process.
- c. Worley, Jr. et al. (U.S. Patent Number 4,713,755) titled "Cache memory consistency control with explicit software instructions" disclosed a method for maintaining memory integrity in a system with a hierarchical memory using a set of explicit cache control instructions. The caches in the system have two status flags, a valid bit and a dirty bit, with each block of information stored. The operating system executes selected cache control instructions to ensure memory integrity whenever there is a possibility that integrity could be compromised.

- d. Polpeka et al. (U.S. Patent Number 6,081,883) titled "Processing system with dynamically allocatable buffer memory" disclosed a scalable computer system has an interconnect bus providing communication links among a host processor and one or more function-specific processors. The host processor provides a single interface to network administrators for maintaining the system. The network processor (NP) shares a single memory image with other processors and has a buffer memory for buffering requests from the network interfaces. The buffer memory has one or more segments, which are dynamically allocatable to different processors. Upon receiving requests for data from the NP, the file storage processor checks the metadata cache to see if a copy of the requested data has been cached in the NP buffer and, if the copy exists in the NP buffer, causing the NP with the data to respond to the request. The resulting scalable computer provides higher data availability, faster access to shared data, and reduced administrative costs.
- 47. Refer to the enclosed PTO-892 for details and complete listing of other pertinent prior art of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tam (Jenny) Phan whose telephone number is (571) 272-3930. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Cuchlinski can be reached on (571) 272-3925.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William Cuchlinski

SPE

Art Unit 2144 (571) 272-3925

tp November 24, 2004